NB4L7210

2.5V/3.3V Differential 2x10 Crosspoint Clock Driver with SDI Programmable Output Selects

The NB4L7210 is a Clock input crosspoint fanout distribution device selecting between one of two input clocks on each of the 10 differential output pairs. A 10 Bit Serial Data Interface programs each output MUX to asynchronously select either Input clock.

CLOCK inputs can accept LVCMOS, LVTTL, LVPECL, CML, or LVDS signal levels and incorporate an internal 50 ohms on die termination resistors. SCLK, SDATA, and SLOAD input can accept single ended LVPECL, CML, LVCMOS, LVTTL signals levels.

SCLK and SDATA inputs operate up to 20 MHz. SLOAD input loads and latches the output select data. The SDATAOUT pin permits cascading multiple devices. Outputs are optimized for minimal output−to−output skew and low jitter.

Features

- Typical Input Clock Frequency > 2 GHz
- 200 ps Typical Rise and Fall Times
- 800 ps Typical Propagation Delay
- Output to Output Skew 150 ps
- Additive RMS Phase Jitter of 0.2 ps
- Operating Range: V_{CC} = 2.375 V to 3.6 V with V_{EE} = 0 V
- Differential LVPECL Output Level (Typ 700 mV Peak−to−Peak)
- Low Profile 8x8 mm, 52 QFN Package
- 10GE WAN: 155.52 MHz / 622.08 MHz
- 10GE LAN: 161.1328 MHz
- These are Pb−Free Devices*

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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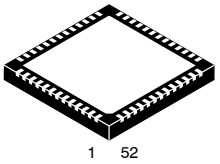
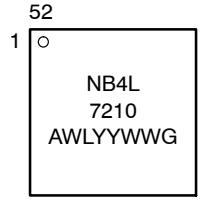


QFN52
MN SUFFIX
CASE 485M

MARKING DIAGRAM*



NB4L7210	= Device Code
A	= Assembly Site
WL	= Wafer Lot
YY	= Year
WW	= Work Week
G	= Pb−Free Package

*For additional marking information, refer to Application Note AND8002/D.

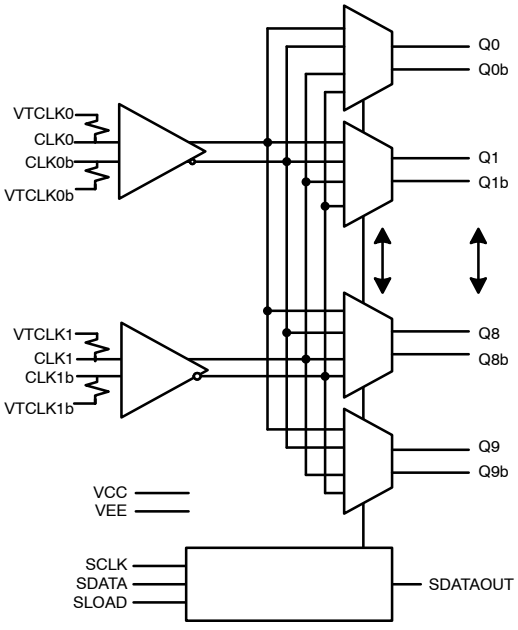


Figure 1. Functional Block Diagram

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 10 of this data sheet.

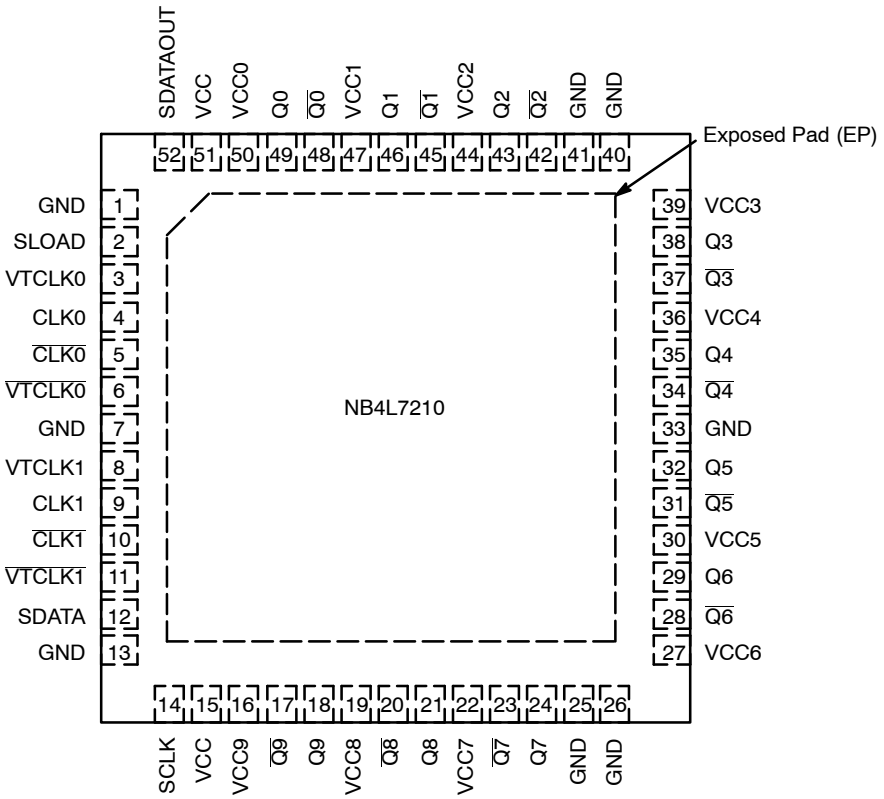


Figure 2. Pin Configuration (Top View)

Table 1. PIN DESCRIPTION

Pin	Name	I/O	Description
1, 7, 13, 25, 26, 33, 40, 41	GND	Supply	Negative Supply pins must be all externally connected to a power supply to guarantee proper operation.
2	SLOAD	LVCMOS, LVTTL	Serial Load and Latch control input pin. Defaults LOW when floating open.
3, 6, 8, 11	VTCLK0, $\overline{\text{VTCLK0}}$, VTCLK1, $\overline{\text{VTCLK1}}$	Termination–	Internal 50 Ohms Termination Resistor connection Pins. In the differential configuration when the input termination pins are connected to the common termination voltage.
4, 9	CLK0, CLK1	Differential LVPECL, CML, or LVDS	CLOCK Input (TRUE). If no signal is applied then the device may be susceptible to self oscillation.
5, 10	$\overline{\text{CLK0}}$, $\overline{\text{CLK1}}$	Differential LVPECL, CML, or LVDS	CLOCK Input (INVERT). If no signal is applied then the device may be susceptible to self oscillation.
12	SDATA	LVCMOS, LVTTL	Serial Data input pin (for BITS 0:9, a “0” selects CLK1, “1” selects CLK 0). Defaults LOW when floating open.
14	SCLK	LVCMOS, LVTTL	Serial Load Clock input pin. Defaults LOW when floating open.
15, 16, 19, 22, 27, 30, 36, 39, 44, 47, 50, 51	VCC, VCC9, VCC8, VCC7, VCC6, VCC5, VCC4, VCC3, VCC2, VCC1, VCC0	Supply	Positive Supply pins must be all externally connected to a power supply to guarantee proper operation.
17, 20, 23, 28, 31, 34, 37, 42, 45, 48	$\overline{\text{Q[9–0]}}$	LVPECL	Output (INVERT)
18, 21, 24, 29, 32, 35, 38, 43, 46, 49	Q[9–0]	LVPECL	Output (TRUE)
52	SDATAOUT	LVCMOS, LVTTL	Serial Data output pin for cascade
Exposed Pad	EP	GND	Exposed Pad. The thermally exposed pad (EP) on package bottom (see case drawing) must be attached to a sufficient heat–sinking conduit for proper thermal operation and must be connected to GND.

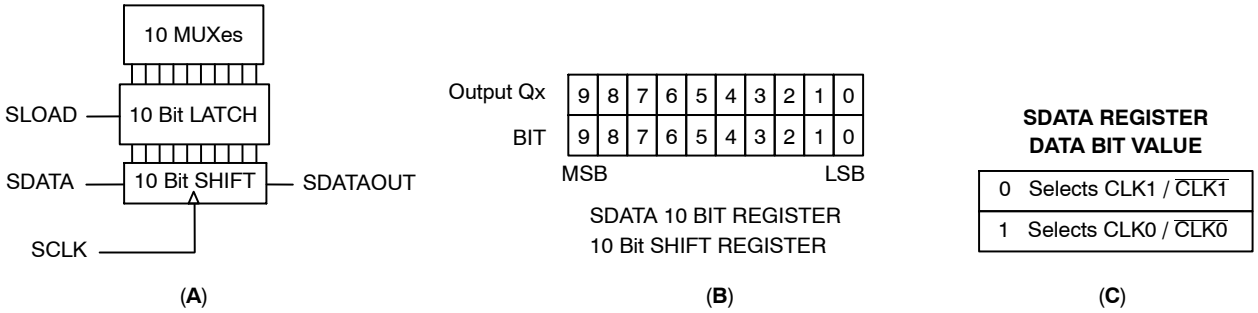


Figure 3. Serial Data Interface

Table 2. ATTRIBUTES

Characteristic		Value
Input Default State Resistors		None
ESD Protection	Human Body Model	> 2 kV
Moisture Sensitivity Pb−Free Package (Note 1)	QFN−52	Level 1
Flammability Rating	Oxygen Index: 28 to 34	UL 94 V−0 @ 0.125 in
Transistor Count		2027
Meets or exceeds JEDEC Spec EIA/JESD78 IC Latchup Test		

1. For additional information, see Application Note AND8003/D.

Table 3. MAXIMUM RATINGS

Symbol	Parameter	Condition 1	Condition 2	Rating	Unit
V_{CC}	Positive Power Supply	GND = 0 V		6.0	V
V_I	Positive Input	GND = 0 V		$GND-0.3 \le V_I \le V_{CC}$	V
I_{IN}	Input Current Through R_T (50 Ω Resistor)	Static Surge		35 70	mA mA
V_{INPP}	Differential Input Voltage			2.5	V
I_{OUT}	Output Current (Q / $\overline{Q}$)	Continuous Surge		25 50	mA
T_A	Operating Temperature Range	QFN−52		−40 to +85	°C
T_{stg}	Storage Temperature Range			−65 to +150	°C
θ_{JA}	Thermal Resistance (Junction−to−Ambient) (Note 2)	0 lfpm 500 lfpm	QFN−52 QFN−52	25 19.6	°C/W °C/W
θ_{JC}	Thermal Resistance (Junction−to−Case)	2S2P (Note 2)	QFN−52	21	°C/W
T_{sol}	Wave Solder Pb−Free			265	°C

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

2. JEDEC standard 51−6, multilayer board − 2S2P (2 signal, 2 power).
3. JEDEC standard multilayer board − 2S2P (2 signal, 2 power) with 8 filled thermal vias under exposed pad.

Table 4. DC CHARACTERISTICS (V_{CC} = 2.375 V to 3.6 V, V_{EE} = 0 V, T_A = −40°C to +85°C (Note 4))

Symbol	Characteristic	Min	Typ	Max	Unit
I_{EED}	GND Supply Current (All Outputs Loaded)	110	150	200	mA
R_{TIN}	Internal Input Termination Resistor	40	50	60	Ω
V_{OH}	Output HIGH Voltage	V_{CC}−1145	V_{CC}−1020	V_{CC}−895	mV
V_{OL}	Output LOW Voltage	V_{CC}−1945	V_{CC}−1820	V_{CC}−1695	mV
I_{IH}	Input HIGH Current (VTx/$\overline{VTx}$ open)		8	150	μA
I_{IL}	Input LOW Current (VTx/$\overline{VTx}$ open)	150	0.1		μA
DIFFERENTIAL INPUTS DRIVEN SINGLE−ENDED (Figures 5, 6)					
V_{th}	Input Threshold Reference Voltage Range (Note 5)	GND +950		V_{CC} − 150	mV
V_{IH}	Single−Ended Input HIGH Voltage	V_{th} + 150		V_{CC}	mV
V_{IL}	Single−Ended Input LOW Voltage	GND		V_{th} − 150	mV
V_{INAMP}	Single−Ended Input Amplitude	300		V_{CC}	
DIFFERENTIAL INPUTS DRIVEN DIFFERENTIALLY (Figures 7, 8)					
V_{CMR}	Input Common Mode Range	GND +950		V_{CC} − 75	mV
V_{IHD}	Differential Input HIGH Voltage	V_{CMR} + 75		V_{CC}	mV
V_{ILD}	Differential Input LOW Voltage	GND		V_{CMR} − 75	mV
V_{ID}	Differential Input Voltage (V_{IHD} − V_{ILD})	150		2400	mV
LVCMOS/LVTTL INPUTS (SCLK, SDATA, SLOAD)					
V_{IH}	Input HIGH Voltage	2.0		V_{CC}	V
V_{IL}	Input LOW Voltage	GND		0.8	V
LVCMOS/LVTTL OUTPUTS (SDATAOUT)					
V_{OH}	Output HIGH Voltage @ I_{OH} = −1.0 mA, R_L = 20 kΩ to GND	2.0	3.2		V
V_{OL}	Output LOW Voltage @ I_{OL} = 1.0 mA, R_L = 20 kΩ to GND		0.25	0.5	V

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

4. Input and Output parameters vary 1:1 with V_{CC}. Outputs loaded with 50 Ω to V_{CC} − 2.0 V (See Figure 16) except SDATAOUT.
5. V_{th} is applied to the complementary input when operating in single−ended mode.

Table 5. AC CHARACTERISTICS (V_{CC} = 2.375 V to 3.6 V, GND = 0 V, T_A = −40°C to +85°C (Note 6))

Symbol	Characteristic	Min	Typ	Max	Unit
V_{OUTPP}	Output Voltage Amplitude @ $V_{INPPmin}$ (See Figure 9) f_{in} = 100 MHz f_{in} = 1 GHz	650 530	800 790	875 960	mV
t_{PLH}, t_{PHL}	Propagation Delay to (See Figure 9) CLK/$\overline{CLK}$ to Qx/$\overline{Qx}$ (Note 7) SCLK to SDATAOUT Measured at 1.5 V	 610 6.5	 725 20	 875 30.8	 ps ns
t_{SKEW}	Duty Cycle Skew (Note 8) Within −Device Skew Device to Device Skew (Note 8)	−5 0 0	2 5 20	10 35 200	ps
ts	Setup Time SDATA to SCLK Measured at 1.5 V SCLK to SLOAD+ Measured at 1.5 V	 −150 1000	 −115		ps
Th	Hold Time SDATA to SCLK	325	345	365	ps
PWmin	Minimum Pulse Width SLOAD	2.0			ns
t_{JIT}(Ø)	RMS Phase Jitter, Integration Range 12 KHz to 20 MHz @155.52 MHz @ 622.08 MHz		 See Fig 10 See Fig 11		fs
t_{JITTER}	TIE Rj (10,000 Cycles) @155.52 MHz @ 622.08 MHz Crosstalk RMS Jitter RMS (1000 Cycles) (Note 9)		1.7 0.63 3.9		ps
V_{INPP}	Input Voltage Swing/Sensitivity (Differential Configuration, measured Single−ended on each input)	150	750	1200	mV
t_r , t_f	Output Risetime and Falltime Qx/$\overline{Qx}$ (20% to 80%) SDATAOUT (0.8 V – 2.0 V)	 120 0.88	 185 10	 260 15	 ps ns

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

6. Measured by forcing V_{INPP} (Typ 750 mV_{PP}) from a 50% duty cycle clock source. Q/$\overline{Q}$ Outputs loaded with 50 Ω to V_{CC} – 2.0 V (See Figure 16). SCLK, SDATA and SLOAD at LOW SDATAOUT loaded 20 kΩ and 15 pF to GND.
7. Measured from the input pair crosspoint to each single output pair crosspoint.
8. Duty cycle skew is measured between differential outputs using the deviations of the sum of T_{pw}− and T_{pw}+.
9. 155.52 MHz @ 750 mV_{PP} input on measured output, 161.13 MHz @ 850 mV_{PP} input on all other others.

Programming Application Information for the SDI

To use the serial port, the SCLK signal samples the information on the SDATA line and indexes the data into a 10 bit shift register (See Figure 3). The register shifts once per rising edge of the SCLK input. The serial input SDATA bits must each meet setup and hold timing to their respective SCLK rising edge as specified in the AC Characteristics section of this document. (See Figure 4)

The SDATA Least Significant Bit (LSB), D0, is indexed in first and the Most Least Significant Bit (LSB), D9, is indexed in last. A Pulse on the SLOAD pin after the SHIFT register is fully indexed (10 clocks) will load and lock the MUX select data values into the Latch register (See Figure 4). For each MUX (Output Q[0:9], a “0” bit value selects CLK1 and a “1” bit value selects CLK 0 (see Figure 3, “C”).

As shown in Figure 4, the SLOAD pulse Low to HIGH level transition transfers the data from the SHIFT register to the LATCH register. The SLOAD Pulse HIGH to LOW level transition will lock the new MUX select data values into the LATCH register. An initial program load cycle is recommended since the 10 bit register will power−up in a random state.

SDATAOUT pin outputs the shift register LSB bit with each SCLK rising edge for porting to the SCLK of the next device in a cascade interconnect only. Cascade operation will require a complete data register loading of all devices to purge the shift registers of power up random state bits.

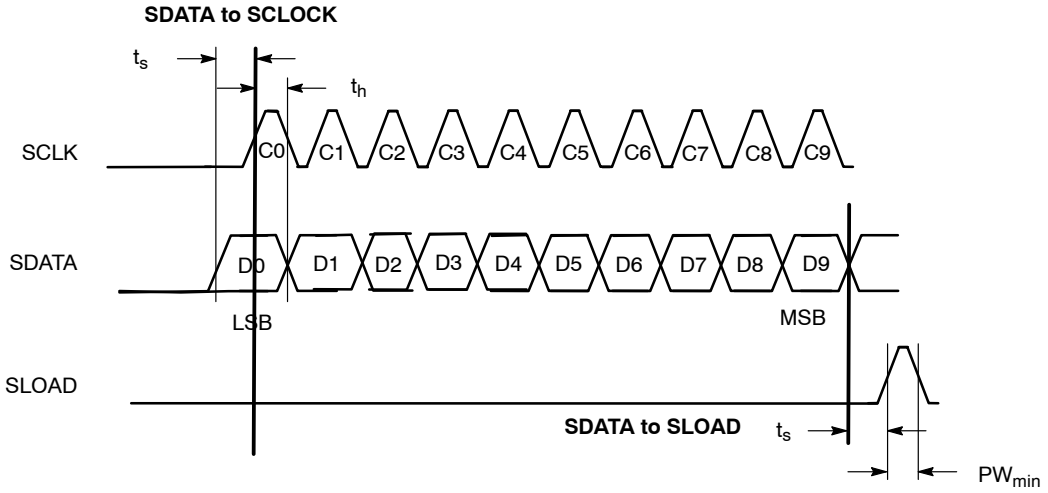


Figure 4. Serial Interface Timing Diagram

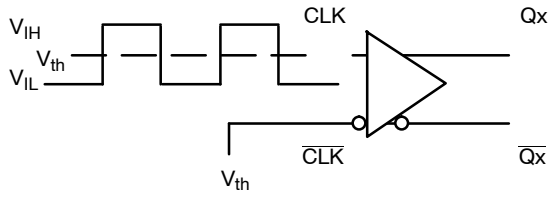


Figure 5. Differential Input Driven Single−Ended V_{th} Schema

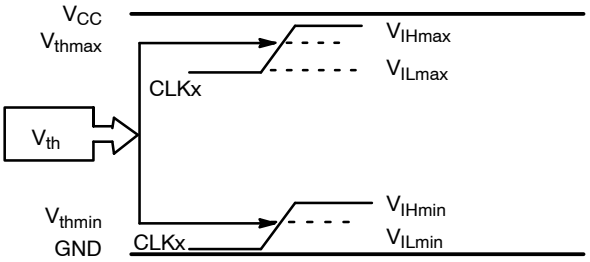


Figure 6. Differential Input Driven Single−Ended V_{th} Diagram

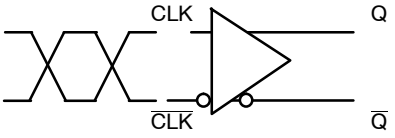


Figure 7. Differential Inputs Driven Differentially

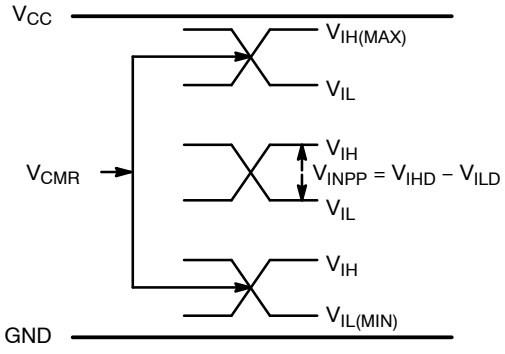


Figure 8. V_{CMR} Diagram

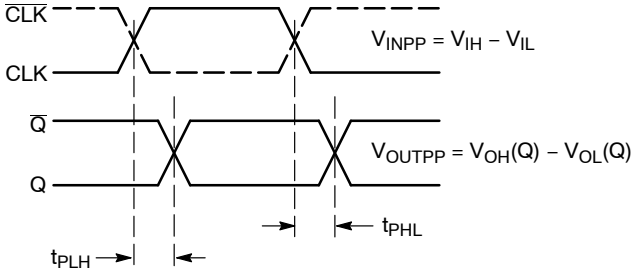


Figure 9. AC Reference Measurement

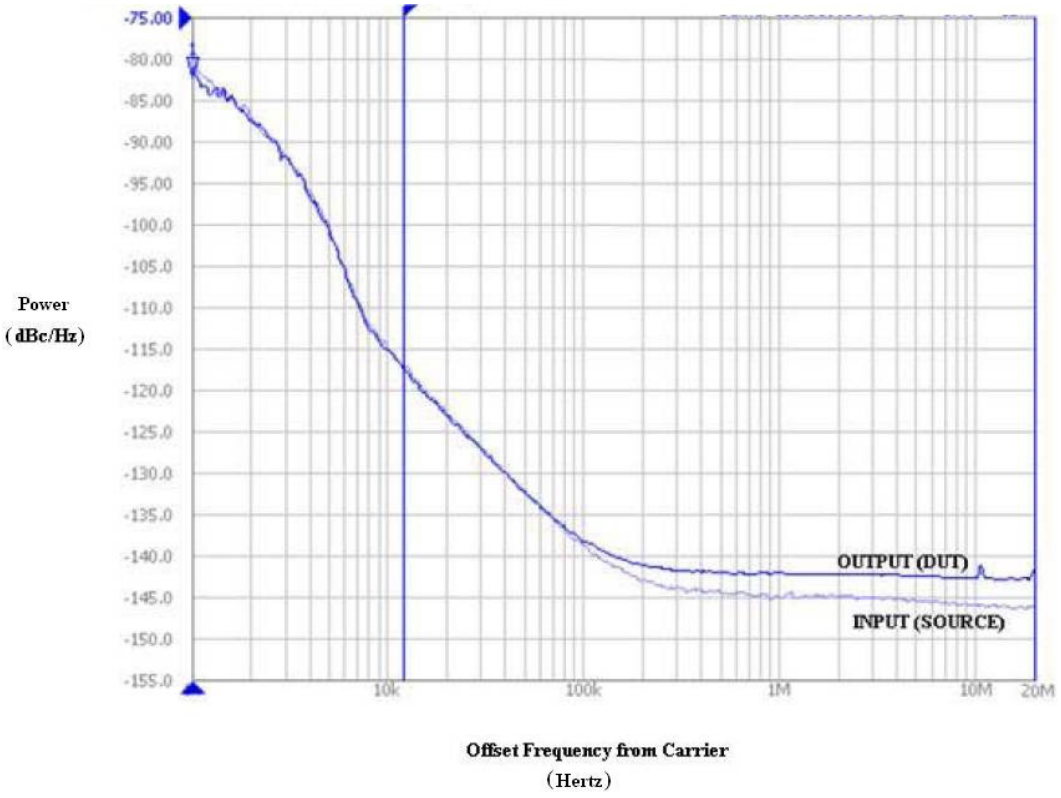


Figure 10. With conditions of an Input (source) noise floor below the NB4L7210 device noise floor, additive Phase Noise with a 155.52 MHz Carrier (Agilent 8665A) is revealed. Note near zero additive Phase Noise below 100 kHz offset. From 100 kHz to 20 MHz additive (residual) integrated phase noise Jitter is about 200 fs RMS.

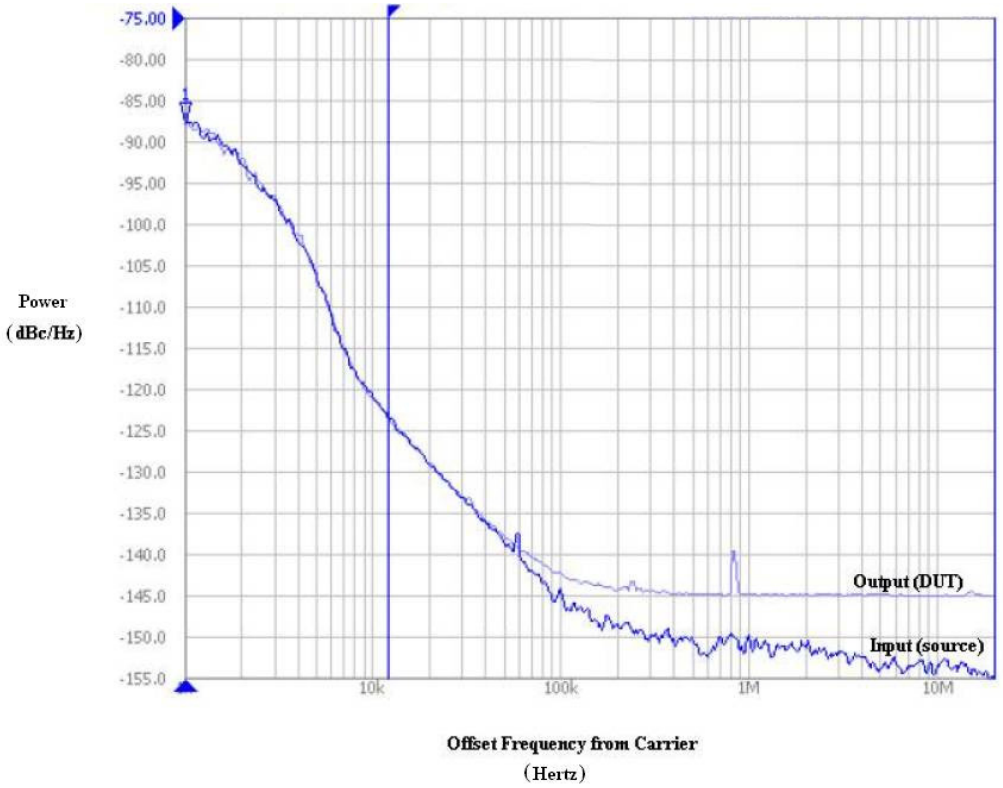


Figure 11. With conditions of an Input (source) noise floor below the NB4L7210 device noise floor, additive Phase Noise with a 622.08 MHz Carrier (Agilent 8665A) is revealed. Note near zero additive Phase Noise below 50 kHz offset. From 50 kHz to 20 MHz additive (residual) integrated phase noise Jitter is about 200 fs RMS.

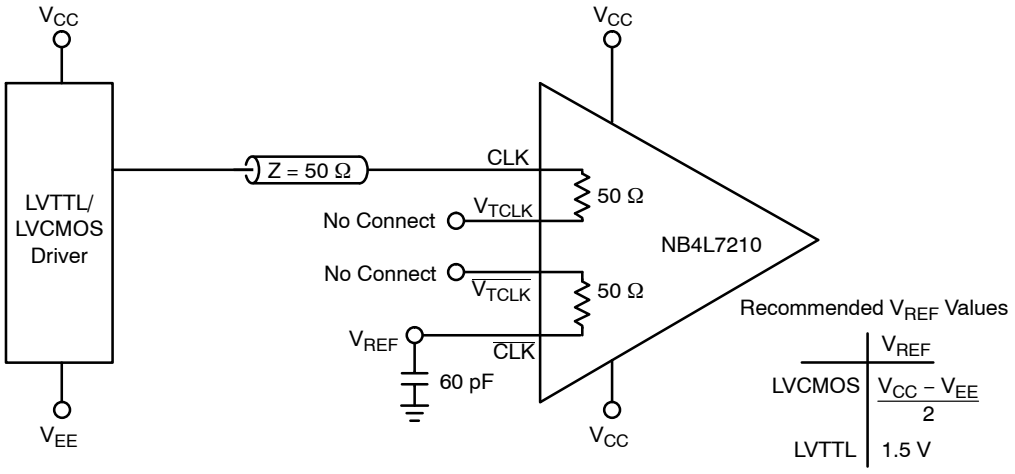


Figure 12. LVCMOS/LVTTL to NB4L7210 Receiver Interface

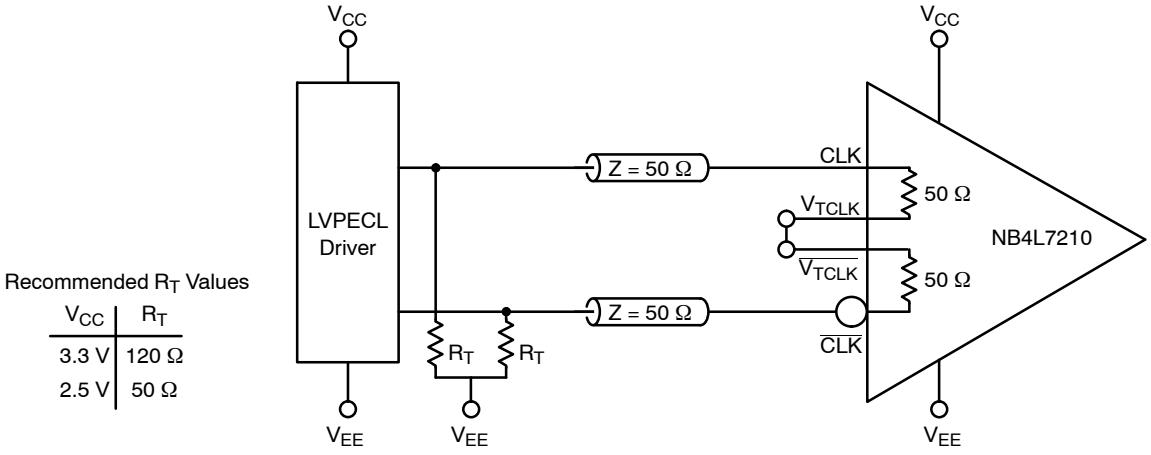


Figure 13. LVPECL to NB4L7210 Receiver Interface

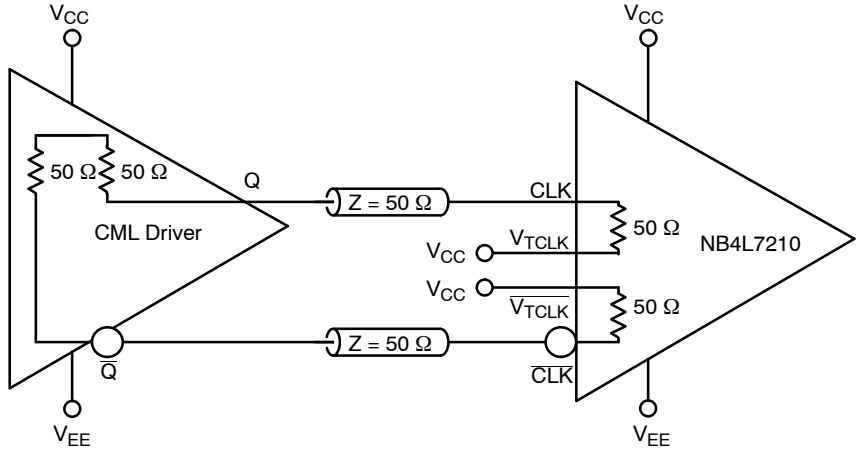


Figure 14. CML to NB4L7210 Interface

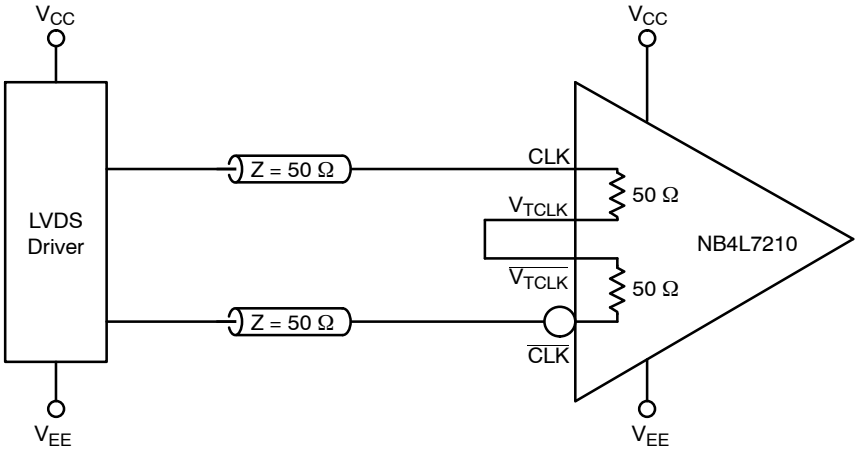


Figure 15. LVDS to NB4L7210 Receiver Interface

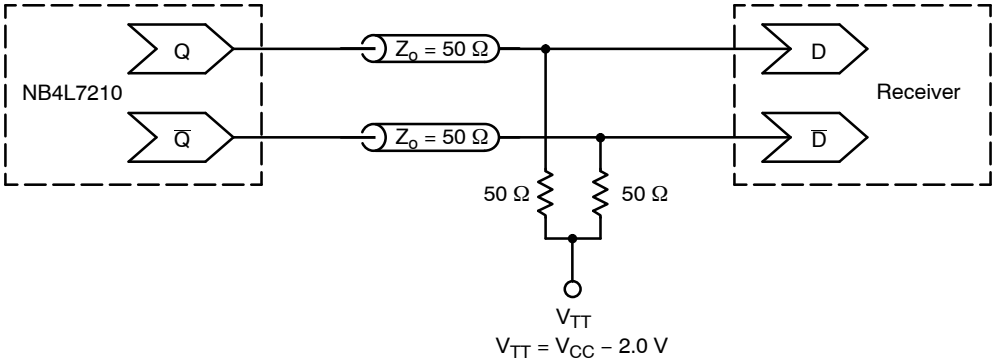


Figure 16. Typical Termination for Output Driver and Device Evaluation (See Application Note AND8020/D – Termination of ECL Logic Devices.)

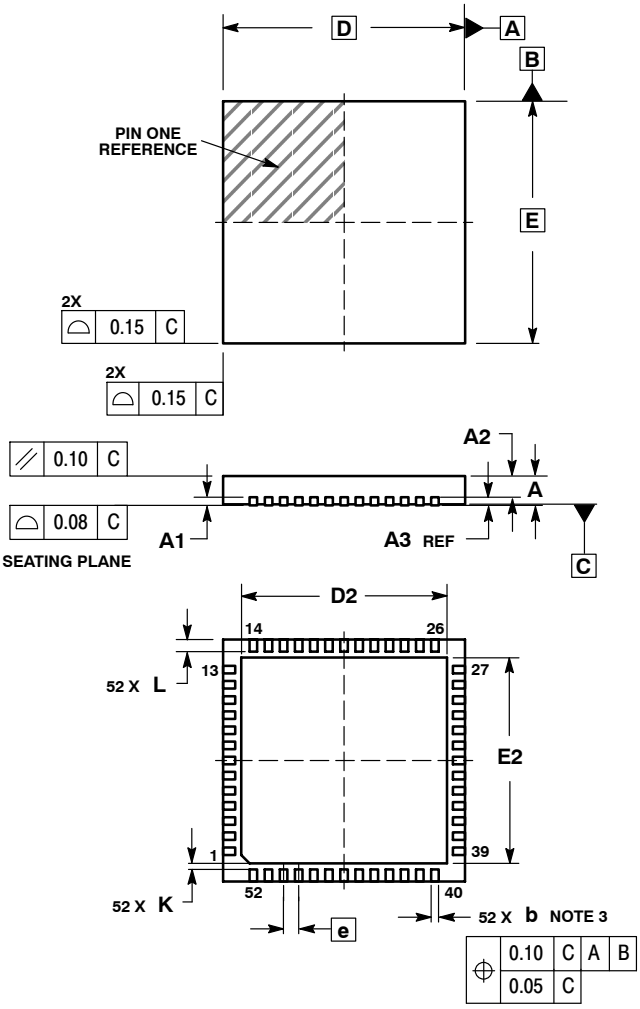
ORDERING INFORMATION

Device	Package	Shipping†
NB4L7210MNG	QFN–52 (Pb–Free)	46 Units / Rail
NB4L7210MNTXG	QFN–52 (Pb–Free)	2000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

PACKAGE DIMENSIONS

52 PIN QFN 8x8
CASE 485M−01
ISSUE B



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.25 AND 0.30 MM FROM TERMINAL.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

	MILLIMETERS	
DIM	MIN	MAX
A	0.80	1.00
A1	0.00	0.05
A2	0.60	0.80
A3	0.20 REF	
b	0.18	0.30
D	8.00 BSC	
D2	6.50	6.80
E	8.00 BSC	
E2	6.50	6.80
e	0.50 BSC	
K	0.20	---
L	0.30	0.50

PUBLICATION ORDERING INFORMATION

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